Using the HT9200A/B DTMF Generator

A/N: HA0037E

Introduction

The program example shows how to use the HT9200A/B.

Using the Driver

→ **Driver Description**

- The program contains the initialisation parameters and both serial and parallel mode transmit data for the HT9200A/B as differentiated in the HT9200A.ASM and the HT9200B.ASM programs.
- If the HT9200A is being used then only the HT9200A.ASM data definitions are used. The INIT_SENDER_SERIAL_9200A, SEND_DATA_SERIAL_9200 subroutines are placed in the related locations in the user program. Note that the data definitions should be modified according to the user hardware circuit.
- If the HT9200B Serial Mode is being used then only the HT9200B.ASM data definitions are used. The INIT_SENDER_SERIAL_9200B, SEND_DATA_SERIAL_9200 subroutines are placed in the related locations in the user program. When using the parallel mode it is important that the data definitions in the HT9200B.ASM, INIT_SENDER_PARALLEL_9200B, SEND_DATA_PARALLEL_9200B subroutines are placed in the correct related location. In the same way the data definitions should be modified according to the user hardware circuit.

→ **Individual Driver Details**

- HT9200ASerial Mode includes 2 sub-routines:
  INIT_SENDER_SERIAL_9200A and SEND_DATA_serial_9200
  INIT_SENDER_SERIAL_9200A:
  Practical Function: Serial Mode initialization program
  Input Parameters: None
  Output Parameters: None
  ROM resources: 6
  RAM Resources: None

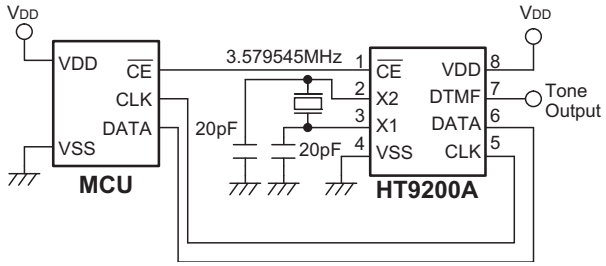
STACK Resources: None
SEND_DATA_serial_9200:
Practical Function: HT9200BSerial Mode Data Transfer Program
Input Parameters: SEND_DATA
Output Parameters: None
ROM Resources: 13
RAM Resources: 2
STACK Resources: None

- HT9200BSerial Mode includes 2 sub-routines:
  INIT_SENDER_SERIAL_9200B and SEND_DATA_serial_9200
  INIT_SENDER_SERIAL_9200B:
  Practical Function: Serial Mode initialiasation program
  Input Parameters: None
  Output Parameters: None
  ROM Resources: 8
  RAM Resources: None
  STACK Resources: None
  SEND_DATA_serial_9200:
  Practical Function: HT9200B Serial Mode Data Transfer Program
  Input Parameters: SEND_DATA
  Output Parameters: None
  ROM Resources: 13
  RAM Resources: 2
  STACK Resources：None
- HT9200B Parallel Mode includes 2 sub-routines:
  INIT_SENDER_PARALLEL_9200B and SEND_DATA_PARALLEL _9200
  INIT_SENDER_PARALLEL _9200B:
  Practical Function: Serial Mode Initialisation
  Input Parameters: SEND_DATA
  Output Parameters: None
  ROM Resources: 9
  RAM Resources: None
  STACK Resources: None
  SEND_DATA_PARALLEL _9200:
  Practical Function: HT9200B Serial Mode Data Transfer Program
  Input Parameters: SEND_DATA
  Output Parameters: None
  ROM Resources: 13
  RAM Resources: 1
  STACK Resources: None
  See program comments in: HT9200A.ASM and HT9200B.ASM

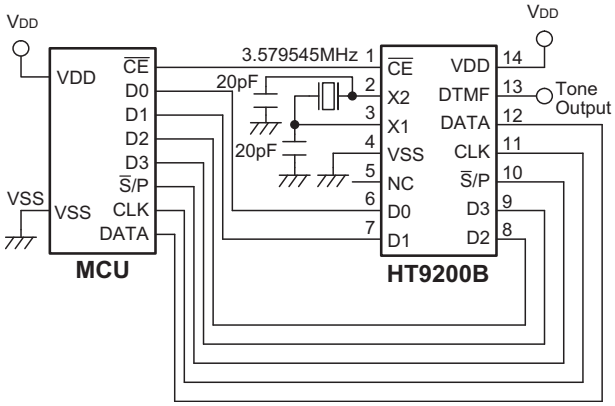
Application Example

Application Circuit

- Serial Mode



- Parallel Mode

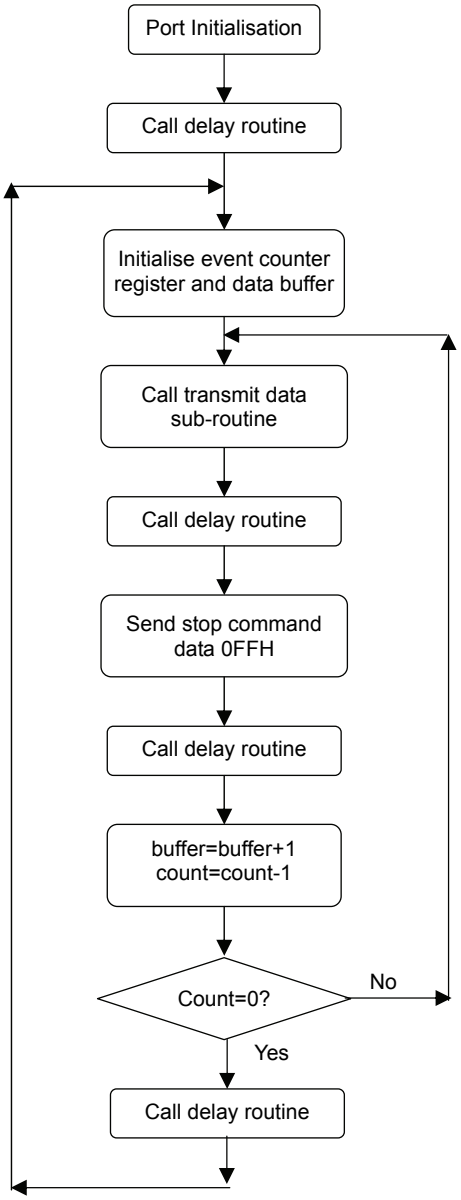


Application Example Program Description

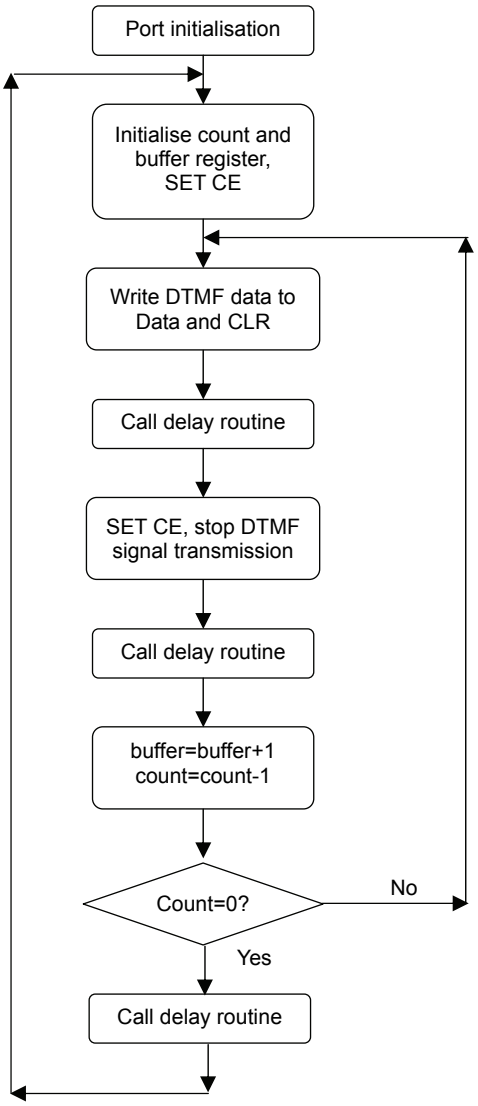
In the present example, the HT48R30A-1 device is used to control the HT9200A/B DTMF generator. There are two methods to generate the DTMF, Serial Mode and Parallel Mode, therefore three macros are defined, SERIAL_MODE_9200A, SERIAL_MODE_9200B and PARALLEL_MODE, which are used according to whethere the serial mode or parallel mode of data is used to generate the DTMF signal. As the HT9200A device only has a Serial Mode and the HT9200B has both Serial and Parallel Mode, a Macro TYPE_MODE is defined, which can according the device type and operating mode execute a conditional assembly. For details consult the HT9200.ASM program

Flowchart

- Serial Mode



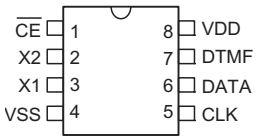
- Parallel Mode



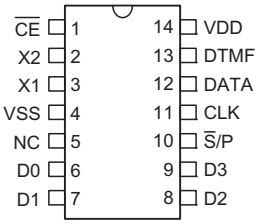
Device Introduction

The HT9200A/B DTMF generator devices are designed to interface easily with MCUs. The devices can generate 16 Dual Tone frequencies and 8 single tone frequencies, which will be transmitted on the DTMF output pin. The HT9200A supplies a Serial Mode of operation while the HT9200B can choose from both Serial or Parallel operating modes. Both devices are applicable for use in a wide range of applications such as emergency call systems, home automation, telephone line control applications, etc.

The HT9200A is supplied in a 8DIP/SOP package, while the HT9200B is supplied in a 14SOP package.



HT9200A
－8 DIP-A/SOP-A



HT9200B
－14 SOP-A

Serial Mode - HT9200A/HT9200B)

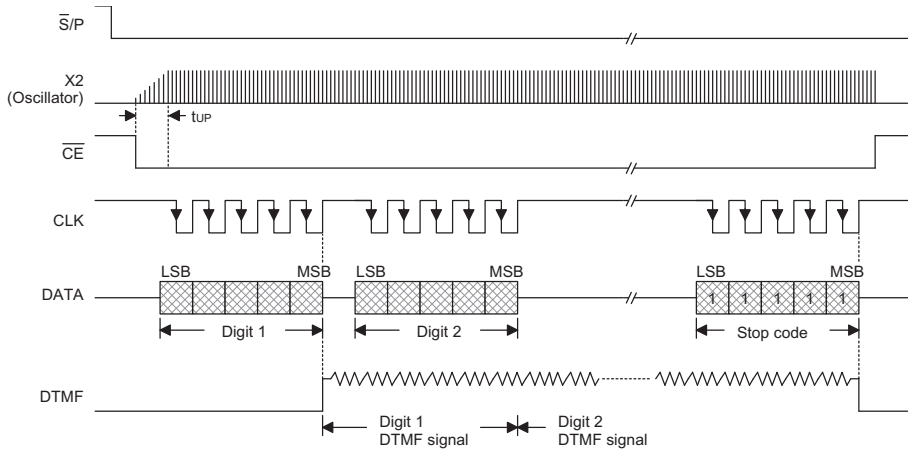
When in the Serial Mode, the HT9200A/B receives its 5-bit data on the DATA pin which is then used to output the required signal on the DTMF pin. This 5-bit data should be provided in the order of D0 to D4. The data must be placed into the output data register before the falling edge of the CLK signal.

The relationship between the Output Frequency and the Serial Data input is as follows:

Digit	D4	D3	D2	D1	D0	Output Frequency (Hz)
1	0	0	0	0	1	697+1209
2	0	0	0	1	0	697+1336
3	0	0	0	1	1	697+1477
4	0	0	1	0	0	770+1209
5	0	0	1	0	1	770+1336
6	0	0	1	1	0	770+1477
7	0	0	1	1	1	852+1209
8	0	1	0	0	0	852+1336
9	0	1	0	0	1	852+1477
0	0	1	0	1	0	941+1336
*	0	1	0	1	1	941+1209
#	0	1	1	0	0	941+1477

Digit	D4	D3	D2	D1	D0	Output Frequency (Hz)
A	0	1	1	0	1	697+1633
B	0	1	1	1	0	770+1633
C	0	1	1	1	1	852+1633
D	0	0	0	0	0	941+1633
—	1	0	0	0	0	697
—	1	0	0	0	1	770
—	1	0	0	1	0	852
—	1	0	0	1	1	941
—	1	0	1	0	0	1209
—	1	0	1	0	1	1336
—	1	0	1	1	0	1477
—	1	0	1	1	1	1633
DTMF OFF	1	1	1	1	1	—

Timing Diagram:



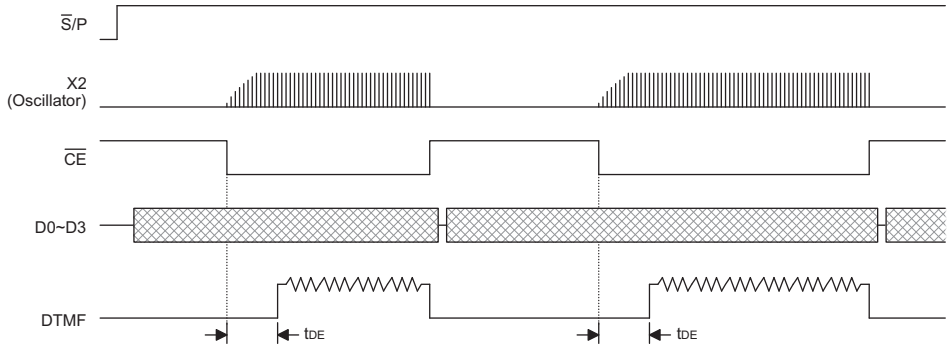
Parallel Mode -- HT9200B only

The HT9200B in addition to its Serial Mode of operation also has a Parallel Mode. When the $\overline{S}$/P pin is high, the HT9200B will be in its Parallel Mode. When in the Parallel Mode the HT9200B uses its D0~D3 input pins to select the required DTMF frequency. When the $\overline{CE}$ pin goes from high to low, the input data will be received. The delay between the $\overline{CE}$ line going low and the generation of the DTMF signal is about 6ms.

The relationship between the Output Frequency and the Parallel inputs is as follows:

Digit	D3	D2	D1	D0	Output Frequency (Hz)
1	0	0	0	1	697+1209
2	0	0	1	0	697+1336
3	0	0	1	1	697+1477
4	0	1	0	0	770+1209
5	0	1	0	1	770+1336
6	0	1	1	0	770+1477
7	0	1	1	1	852+1209
8	1	0	0	0	852+1336
9	1	0	0	1	852+1477
0	1	0	1	0	941+1336
*	1	0	1	1	941+1209
#	1	1	0	0	941+1477
A	1	1	0	1	697+1633
B	1	1	1	0	770+1633
C	1	1	1	1	852+1633
D	0	0	0	0	941+1633

Timing Diagram:



Note: The data (D0~D3) should be ready before the $\overline{CE}$ becomes low.